IN THE SPECIFICATION

Please amend the paragraph at page 11, lines 2-25, as follows:

A location of a defective pixel is previously detected during inspection of the image sensor 11, and defect correction data DCD containing information about the location of the defective pixel is recorded on the ROM 19 (Fig. 1). The defect correction data DCD is transferred by the DMAC 17 from the ROM 19 to the SPU 12 for each pixel at a time of input of a G signal to the defective pixel correction circuit 49, and is received by an input control circuit 63. It is additionally noted that the defect correction data DCD is not always transferred directly from the ROM 19 by a DMA method. Alternatively, the defect correction data DCD may be once copied into the RAM 18, and then subjected to DMA transfer. The input control circuit 63 drives a FIFO circuit 63a to perform buffering on the received defect correction data DCD, and thereafter sends the defect correction data DCD to the timing generator 52. The timing generator 52 generates the control signal TS based on the defect correction data DCD, and sends the control signal TS to the defective pixel correction circuit 49 and other defective pixel correction circuits 50 and 51 which will be ~~descried~~ described later. Thus, the three defective pixel correction circuits 49, 50 and 51 correct signals associated with one and the same pixel at the same time. It is noted that the defect correction data DCD need not necessarily be previously stored in a memory such as the ROM 19 or the RAM 18, to be transferred from the memory by a DMA method. Alternatively, the defect correction data DCD may be stored in a register included in the timing generator 52, for example. Further alternatively, the defect correction data DCD stored in a memory such as the ROM 19 may be transferred by the CPU without use of DMA method, if the CPU 14 has a handling capability enough to do so. In short, storage location of the defect correction data DCD and a method for transferring the defect correction data DCD are not limited to any specific location and method in the present invention.

Please amend the paragraph at page 19, lines 10-21, as follows:

On the other hand, the Y signal and the ~~UVsignal~~ UV signal output from the separation circuit 20 are joined and transmitted as a 16-bit YUV422 signal to the "1"-st terminal of the selector 57 (Fig. 3). The selector 57 outputs either a signal output from the selector 56 in the preceding stage or the YUV422 signal, to the output control circuit 58. The output control circuit 58 outputs a signal which should be subjected to DMA transfer, to the bus 16. Hence, by driving the selector 57 to select the "1"-st terminal, it is possible to accomplish output of the Y signal, the U signal and the V signal (YUV444 signal) to the RPU 13, in parallel with DMA transfer of the YUV422 signal on which no processing has been performed to another module. Since the YUV422 signal is not oversampled, an amount of transferred data for the YUV422 signal is smaller than an amount of transferred data for the YUV444 signal, which advantageously reduces a band occupied by the bus 16.

Please amend the paragraph at page 24, line 22 to page 25, line 2, as follows:

The first, second and third selectors 94, 95 and 96 receive 2-bit selection control signals TCPHR [1:0], TCPHG [1:0] and TCPHB [1:0], respectively, from the CPU 14. Then, each of the selectors selects one terminal among the "0"-th, "1"-st, "2"-nd, and "3"-rd ~~and "4"-th~~ terminals thereof depending on a value of the received 2-bit selection control signal, and outputs a signal received by the selected terminal, to the register.